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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	09/784,419
Filing Date	February 15, 2001
First Named Inventor	Cao, Jun
Art Unit	2633
Examiner Name	Christina Y. Leung
Attorney Docket Number	019717-001210US

U.S. PATENT DOCUMENTS

Examiner	Cite No.[1]	Document Number Number Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
DP	AA	US-4,535,459	08-13-1985	Hogge, Jr.	
DP	AB	US-5,301,196	04-15-1994	Ewen et al.	
DP	AC	US-09/955,693	filed 09-18-2001	Jun Cao	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] Number[4] Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
	AD					
	AE					

OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials *	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
DP	AF	C.R. HOGGE, JR., "A Self Correcting Clock Recovery Circuit", IEEE Journal of Lightwave Technology, vol. LT-3, no. 6, December 1985	
	AG	E. MULLNER, "A 20 Gb/s Parallel Phase Detector and Demultiplexer Circuit in a Production Silicon Bipolar Technology with fT=25 GHz", Proc. IEEE BCTM, pp. 43-45, Oct. 1996	
	AH	M. RAU et al., "Clock/Data Recovery PLL Using Half-Frequency Clock", IEEE Journal of Solid-State Circuits, vol. 32, no. 7, July 1997	
	AI	K. NAKAMURA et al., "A 6 Gb/s CMOS Phase Detecting DEMUX Module Using Half-Frequency Clock", IEEE 1998 Symposium on VLSI Circuits Digest of Technical Papers	
	AJ	M. WURZER et al., "40-Gb/s Integrated Clock and Data Recovery Circuit in a Silicon Bipolar Technology", IEEE BCTM 8.1, 1998	
	AK	JAFAR SAVOJ et al., "A 10-Gb/s CMOS Clock and Data Recovery Circuit", IEEE 2000 Symposium on VLSI Circuits Digest of Technical Papers	

Examiner Signature		Date Considered	2/17/04

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] Unique citation designation number. [2] Applicant is to place a check mark here if English language Translation is attached.

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DP	AA	US-6,121,804	09-19-2000	Bryan et al.	

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DP	AB	PCT	WO 01/06696 ✓	01-25-2001	Chang et al.		☐
DP	AC	PCT	WO 01/63767 ✓	08-30-2001	Green		☐

Examiner Signature	DPuegen	Date Considered	2/17/04

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